SUMMARY

This document is the official specification of the Chameleon POD. The specification are corresponding with the schematic version v1.2 of the Chameleon POD. In this document, you will discover all necessary features of the Chameleon POD that you need to know before developing your own project based on it. Copyright © Amontec, 2002. All rights reserved.

Extend the capability of your Parallel Port with our pre-defined configurations or with your own custom application in a fraction of time.
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1 INTRODUCING THE FEATURES

The Chameleon POD is based on programmable logic and is built in a very small format. It will allow you to implement quickly small active state-machines like parallel-to-serial protocols.

The Chameleon POD has a full compatibility with the IEEE 1284 standard, including SPP mode (Standard Parallel Port), EPP mode (Enhanced Parallel Port) and ECP Mode (Extended Capabilities Port).

1.1 THE CHAMELEON POD USAGES:

- The Chameleon POD will be used for Xilinx Coolrunner CPLD rapid prototyping. As a stand-alone application or as a Parallel Port application the Chameleon POD will provide an exclusive flexibility and smoothness.

- The first advantage of the Chameleon POD is the FREE configurations that you can download on the Amontec website (http://www.amontec.com). In the prototyping world, we need JTAG Emulators or JTAG Download Cables every day. The power of the Chameleon POD is to integrate all the most popular Parallel Port JTAG Download Cables. The Chameleon POD is becoming the universal JTAG POD or JTAG Emulator.

Since the Chameleon POD can be directly configured and driven by the Parallel Port of any computer and without additional cable, it will allow you to give many new custom functions to your Parallel Port. For example, with the same hardware, you can configure the Chameleon Board for obtaining a Direct Digital Synthesizer (DDS), a Pseudo-Wiggler JTAG POD for debugging your favorite ARM processor, a Pseudo-XilinxCableIII JTAG POD for downloading your favorite FPGA, or for obtaining your own custom configuration.
2 BLOCK DIAGRAM

This following block diagram describes the capabilities of the Chameleon POD board.

![Block Diagram](image)

Figure 1: Chameleon POD Block diagram

Note: This block diagram shows you the positions of the Slide Switch corresponding with the board modes.
3 MOST IMPORTANT ONBOARD COMPONENTS

The most important onboard components of the Chameleon POD are:

- U1: A Coolrunner CPLD (programmable logic, 5V and 3.3V tolerant I/O pins)
- Q1: A 32MHz Crystal Oscillator
- P1: A D-Sub 25 pin male Connector (computer side)
- P2: A D-Sub 25 pin female Connector (for user side and for power source)
- P3: A power Jack Connector
- S1: A Slide Switch allowing the mode selection ('configure' mode or 'use' mode)
- LED1: A red LED for custom uses
- LED2: A yellow LED for configuration mode signalization
- LED3: A green LED for power signalization
- A DC-DC Linear Regulator allowing the Chameleon board to be used in different power level environments.

Note: the Chameleon POD Board comes with optional colored flying-lead cables allowing a rapid use of the different configurations.
4 CHAMELEON POD SPECIFICATION

4.1 HOW TO POWER THE CHAMELEON POD

Since there is no dedicated power pin on the Parallel Port of your computer, you need to power the POD from an external source. There are three possibilities to power the POD:

- via the Power Jack Connector (P3)
- via the pin number 1 or the pin number 13 of the D-Sub 25 pin female Connector (P2).

An onboard protection circuit prevents you about a dual power source use. When the Power Jack connector is plugged, then the other power sources are automatically disconnected.

The POD has an onboard 3.3V 200mA linear regulator. The regulator can drive a current about 200mA.

4.1.1 POWERING THE POD VIA THE POWER JACK CONNECTOR (P3)

This possibility to power the POD has the advantage to protect it from a polarity error of your power source. But consequently, the POD will not work at 3.3V, but only in a power range about 4V to 9V.

When using a transformer, you need to make sure about its specification:

- Output Voltage Range: 4V to 9V
- Minimum Current: 200mA
- Inner diameter of the plug: 1.8mm

Plug polarity:

When the POD is correctly powered, the green LED (LED3) will light.

4.1.2 POWERING THE POD VIA THE PIN NUMBER 1 OR/AND VIA THE PIN NUMBER 13 OF THE D-SUB FEMALE CONNECTOR

This possibility to power the board must be used CAUTIOUSLY, because the power polarity is not checked. But it has the advantage to power the board in a 3.3V to 8.3V range.

This possibility will be appropriate if you use the Chameleon board like a bridge between the computer and a third board. For example, for a JTAG configuration, the power is often available in the JTAG connector of the third board with a value 3.3V or 5V and can be used as it is.
4.1.3 RESUMING

<table>
<thead>
<tr>
<th>Powering the board</th>
<th>Polarity check</th>
<th>Power range</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Via the Power Jack Connector</td>
<td>YES</td>
<td>4V to 9V</td>
<td></td>
</tr>
<tr>
<td>Via pin 1 or pin 13 of the D-Sub female connector (user side)</td>
<td>NO</td>
<td>3.3V to 8.3V</td>
<td>Must be used CAUTIOUSLY</td>
</tr>
</tbody>
</table>

Table 1: How to power the POD
### 4.2 P1: D-SUB MALE CONNECTOR (COMPUTER SIDE)

In the following table, you find the pinout description of the D-Sub 25 pin male connector corresponding with the computer side. We have added the Parallel Port signal name (in SPP mode).

<table>
<thead>
<tr>
<th>Pin No (D-Sub 25 pin male connector)</th>
<th>SPP Signal</th>
<th>SPP Direction</th>
<th>To CPLD Pin No</th>
<th>CPLD pin direction possibilities</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>nStrobe</td>
<td>In/Out</td>
<td>P20</td>
<td>In/Out</td>
</tr>
<tr>
<td>2</td>
<td>Data0</td>
<td>Out (In)</td>
<td>P62</td>
<td>In/Out(TCK)</td>
</tr>
<tr>
<td>3</td>
<td>Data1</td>
<td>Out (In)</td>
<td>P4</td>
<td>In/Out(TDI)</td>
</tr>
<tr>
<td>4</td>
<td>Data2</td>
<td>Out (In)</td>
<td>P15</td>
<td>In/Out(TMS)</td>
</tr>
<tr>
<td>5</td>
<td>Data3</td>
<td>Out (In)</td>
<td>P32</td>
<td>In/Out</td>
</tr>
<tr>
<td>6</td>
<td>Data4</td>
<td>Out (In)</td>
<td>P33</td>
<td>In/Out</td>
</tr>
<tr>
<td>7</td>
<td>Data5</td>
<td>Out (In)</td>
<td>P40</td>
<td>In/Out</td>
</tr>
<tr>
<td>8</td>
<td>Data6</td>
<td>Out (In)</td>
<td>P42</td>
<td>In/Out</td>
</tr>
<tr>
<td>9</td>
<td>Data7</td>
<td>Out (In)</td>
<td>P45</td>
<td>In/Out</td>
</tr>
<tr>
<td>10</td>
<td>nAck</td>
<td>In</td>
<td>P48</td>
<td>In/Out</td>
</tr>
<tr>
<td>11</td>
<td>Busy</td>
<td>In</td>
<td>P73</td>
<td>In/Out(TDO)</td>
</tr>
<tr>
<td>12</td>
<td>Paper-Out / PaperEnd</td>
<td>In</td>
<td>P52</td>
<td>In/Out</td>
</tr>
<tr>
<td>13</td>
<td>Select</td>
<td>In</td>
<td>P54</td>
<td>In/Out</td>
</tr>
<tr>
<td>14</td>
<td>nAuto-Linefeed</td>
<td>In/Out</td>
<td>P21</td>
<td>In/Out</td>
</tr>
<tr>
<td>15</td>
<td>nError / nFault</td>
<td>In</td>
<td>P23</td>
<td>In/Out</td>
</tr>
<tr>
<td>16</td>
<td>nInitialize</td>
<td>In/Out</td>
<td>P25</td>
<td>In/Out</td>
</tr>
<tr>
<td>17</td>
<td>nSelect-Printer / nSelect-In</td>
<td>In/Out</td>
<td>P29</td>
<td>In/Out</td>
</tr>
<tr>
<td>18-25</td>
<td>Ground</td>
<td>Gnd</td>
<td>Gnd</td>
<td>Gnd</td>
</tr>
</tbody>
</table>

Table 2: P1: D-Sub male connector pinout (computer side)
4.3 P2: D-SUB FEMALE CONNECTOR (USER SIDE)

In the following table, you find the pinout description of the D-Sub 25 pin female connector corresponding with the user side.

<table>
<thead>
<tr>
<th>Pin No (D-Sub 25 pin female connector)</th>
<th>Signal Name</th>
<th>To CPLD Pin No</th>
<th>CPLD pin direction possibilities</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Power In</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>GIO_02</td>
<td>P99</td>
<td>In/Out</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>GIO_03</td>
<td>P97</td>
<td>In/Out</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>GIO_04</td>
<td>P93</td>
<td>In/Out</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>GIO_05</td>
<td>P92</td>
<td>In/Out</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>GIO_06</td>
<td>P84</td>
<td>In/Out</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>GIO_07</td>
<td>P83</td>
<td>In/Out</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>GIO_08</td>
<td>P81</td>
<td>In/Out</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>GIO_09</td>
<td>P80</td>
<td>In/Out</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>GIO_10</td>
<td>P79</td>
<td>In/Out</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>GIO_11</td>
<td>P75</td>
<td>In/Out</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>GIO_12</td>
<td>P71</td>
<td>In/Out</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>Power In</td>
<td>-</td>
<td>-</td>
<td>(1) Input Power 3.3V to 8.3V</td>
</tr>
<tr>
<td>14</td>
<td>GIO_14</td>
<td>P100</td>
<td>In/Out</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>GIO_15</td>
<td>P98</td>
<td>In/Out</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>GIO_16</td>
<td>P96</td>
<td>In/Out</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>GIO_17</td>
<td>P94</td>
<td>In/Out</td>
<td></td>
</tr>
<tr>
<td>18-25</td>
<td>Ground</td>
<td>Gnd</td>
<td>Gnd</td>
<td></td>
</tr>
</tbody>
</table>

Table 3: P2: D-Sub female connector pinout (user side)

Note: (1) Read the section ‘How to power the Chameleon POD board’ of this document.
In the above table, we did not define the Signal Names corresponding with the Inputs/Outputs of the CPLD, because these Signal Names will depend on the typical configuration of the Chameleon POD. These signals are viewed as General IOs. An application note will be written for each configuration with a specific table introducing the specific Signal Names.

4.4 S1: THE ONBOARD SLIDE SWITCH

The Slide Switch is the most important component of this board. It allows you to choose the mode of the Chameleon POD.

When the Slide Switch is pushed to the computer side, the Chameleon POD Board is in its configuration mode. In this mode, the JTAG port of the CPLD is enabled and the PORT_EN signal is in a high level logic. You can download the new configuration of the CPLD via the Parallel Port of any computer. Amontec supplies a Software Development Kit allowing the download of the new CPLD configuration from any Windows OS.

But on the other hand, when the Slide Switch is pushed to the user side (D-Sub female connector), the chameleon POD is in the ‘use’ mode. In this mode, the dedicated JTAG pins of the CPLD can be use as general I/Os. The PORT_EN signal of the CPLD is in a low level logic.

More, for specific applications, the PORT_EN signal can be directly controlled by the CPLD via the pin number 6. In fact, in the last generation of the Chameleon POD, we have added an external ‘OR’ gate (TinyLogic) allowing the control of the PORT_EN signal state via the Slide Switch or via the pin number 6 of the CPLD.

4.4.1 PIN NUMBER 6 OF THE CPLD: AN OUTPUT FOR THE CPLD

When you are developing a custom application of the CPLD, verify that the pin number 6 of the CPLD is driven by a low level logic. For this effect, we have added an external pull-up resistor on the pin number 6 of the CPLD. If this pin number 6 is in a tristates or a high level logic, the PORT_EN of the CPLD will ever stay enabled. Refer to the schematic for a complete understanding of this mechanism.

4.4.2 PIN NUMBER 12 OF THE CPLD: AN INPUT FOR THE CPLD

When you are developing an application on the Chameleon POD, the input pin number 12 of the CPLD relates the Slide Switch state. This pin number 12 must be viewed as an input for all configuration of the CPLD. In the configuration mode, this input pin will receive a high level logic. Note, in most cases, we didn’t need to use this input pin.

4.5 THE THREE ONBOARD LEDS

To make easy the use of the Chameleon POD, the board is equipped by three onboard LEDs.

4.5.1 GREEN LED: POWER LED

The green LED will stay in an ON state (lighting) while the board is correctly powered. This LED can be called ‘Power LED’.
4.5.2 YELLOW LED: CONFIGURATION LED

The yellow LED indicates that the board is in his ‘configuration mode’. In other words, this LED is in an ON state (lighting) when the Slide Switch is pushed to the computer side (DSUB male connector side). After pushing the Slide Switch in the ‘use’ mode, this LED will return in an OFF state. Also the Chameleon POD board will be ready to use in its specific configuration. In other word, when the yellow LED is lighting, the JTAG port of the CPLD is enabled and you can load a new configuration of the CPLD. We remember that when the yellow LED is in his OFF-state, the JTAG port of the CPLD is disabled and you can use the specific JTAG pins as general I/o.

4.5.3 RED LED: USER LED

The red LED is a ‘free of use’ LED and is connected directly to the CPLD on the pin number 71. This LED can be called ‘User LED’.

4.6 THE ONBOARD QUARTZ CRYSTAL

An onboard 32Mhz Quartz Crystal (+- 50ppm) is directly connected to the input pin number 90 of the CPLD. This Quartz Crystal will allow you to implement your synchronous state machine in the CPLD.

Note: the pin number 85 (OUT) and the pin number 87 (IN3/CLK3) of the CPLD are connected together. This will allow to generate a custom clock signal in the CPLD, and to associate this new clock to the Global Clock Buffer corresponding with the pin number 87 (IN3/CLK3). You easily understand that the pin number 85 will be used as an output for the CPLD, and the pin number 87 as an input.

4.7 THE CPLD: XILINX COOLRUNNER PIN XCR3128XL –VQ100

A CPLD is a programmable logic device. On the Chameleon POD, we have installed a Xilinx CPLD belonging to the Coolrunner family. The exact type of this CPLD is the XCR3128XL –VQ100. Also, the Chameleon board schematic is fully compatible for a XCR3064XL –VQ100 use.

The XCR3128XL is a 3.3V, 128-macrocell CPLD targeted at power sensitive designs that require leading edge programmable logic solutions. A total of four function blocks provide 1,600 usable gates. Pin-to-pin propagation delays are 6.0 ns with a maximum system frequency of 145 MHz. The XCR3128XL has 5V tolerant I/O pins with 3.3V core supply.

For more details about the XCR3128XL CPLD visit the product page of the Xilinx website (http://www.xilinx.com).
4.7.1 CONSTRAINT FILE EXAMPLE (.UCF)

When you are developing an application on the Chameleon POD, you have to write an .ucf constraint file describing the pinning of your CPLD. This .ucf constraint file is used when you are doing the Place & Route of your own HDL application (see about the freeware Xilinx Webpack on www.xilinx.com).

For rapid prototyping of your new application, we give you a generic .ucf file example:

(Just do a ‘copy-paste’ from this document to your own ASCII .ucf constraint file)

```
# Constraint: UCF file for CPLD on Chameleon POD (v1.2)
#
## Rel. prj.: Generic project of the Chameleon POD
## Devicr: XCR3128XL
## Package: VQ100
## Authors: Laurent Gauch 23.06.2002
## Company: Amontec ( http://www.amontec.com )
## Note: for EDIF netlist replace '<' by '(' and ')' by '>
#
## PAD ATTRIBUTE OF D-SUB MALE CONNECTOR (COMPUTER SIDE / PARALLEL PORT)
#
NET strobe_b LOC = "P20" ; # pin no 01 of the D-Sub male connector
NET data<0> LOC = "P62" ; # pin no 02 of the D-Sub male connector
NET data<1> LOC = "P04" ; # pin no 03 of the D-Sub male connector
NET data<2> LOC = "P15" ; # pin no 04 of the D-Sub male connector
NET data<3> LOC = "P32" ; # pin no 05 of the D-Sub male connector
NET data<4> LOC = "P33" ; # pin no 06 of the D-Sub male connector
NET data<5> LOC = "P40" ; # pin no 07 of the D-Sub male connector
NET data<6> LOC = "P42" ; # pin no 08 of the D-Sub male connector
NET data<7> LOC = "P45" ; # pin no 09 of the D-Sub male connector
NET ack_b LOC = "P48" ; # pin no 10 of the D-Sub male connector
NET busy LOC = "P73" ; # pin no 11 of the D-Sub male connector
NET paperend LOC = "P52" ; # pin no 12 of the D-Sub male connector
NET selectin LOC = "P54" ; # pin no 13 of the D-Sub male connector
NET autofd_b LOC = "P21" ; # pin no 14 of the D-Sub male connector
NET error_b LOC = "P23" ; # pin no 15 of the D-Sub male connector
NET init_b LOC = "P25" ; # pin no 16 of the D-Sub male connector
NET select_b LOC = "P29" ; # pin no 17 of the D-Sub male connector

## PAD ATTRIBUTE OF D-SUB FEMALE CONNECTOR (USER SIDE)
#
NET gio_02 LOC = "P99" ; # pin no 02 of the D-Sub female connector
NET gio_03 LOC = "P97" ; # pin no 03 of the D-Sub female connector
NET gio_04 LOC = "P93" ; # pin no 04 of the D-Sub female connector
NET gio_05 LOC = "P92" ; # pin no 05 of the D-Sub female connector
NET gio_06 LOC = "P84" ; # pin no 06 of the D-Sub female connector
NET gio_07 LOC = "P83" ; # pin no 07 of the D-Sub female connector
NET gio_08 LOC = "P81" ; # pin no 08 of the D-Sub female connector
NET gio_09 LOC = "P80" ; # pin no 09 of the D-Sub female connector
NET gio_10 LOC = "P79" ; # pin no 10 of the D-Sub female connector
NET gio_11 LOC = "P75" ; # pin no 11 of the D-Sub female connector
NET gio_12 LOC = "P71" ; # pin no 12 of the D-Sub female connector
NET gio_14 LOC = "P100" ; # pin no 14 of the D-Sub female connector
NET gio_15 LOC = "P98" ; # pin no 15 of the D-Sub female connector
NET gio_16 LOC = "P96" ; # pin no 16 of the D-Sub female connector
```
NET gio_17 LOC = "P94" ; # pin no 17 of the D-Sub female connector
#
# PAD ATTRIBUTE OF SUPPLEMENTARY PINS (CLOCK, CONTROL, STATUS)
#
NET clk LOC = "P90" ; # onboard 32MHz Quartz Crystal
NET clkgen_out LOC = "P85" ; # connected to clkgen_in
NET clkgen_in LOC = "P87" ; # driven by clkgen_out
NET user_led LOC = "P69" ; # onboard red LED
NET port_en_flag LOC = "P12" ; # IN: '1'=JTAG enabled, '0'=JTAG disabled
NET port_ctrl LOC = "P06" ; # OUT: 'Z' to enable JTAG , '0' to disable JTAG
## NOTE : In normal use, the port_ctrl need to be driven by a low level logic.
## port_ctrl signal has an onboard pull-up resistor.
#
# PULLUP DESCRIPTION (IF NEEDED)
#
# NET your_netname PULLUP;
#
## END OF .UCF
##
5 AMONTEC, YOUR FPGA DESIGN PARTNER

Most hardware designs are targeted at systems that have a real-time response requirement. Amontec has over 4 years experience developing hardware for real time applications. Time to market considerations require Early Hardware Prototypes for software development and verification. Product development tradeoffs include:

1) Build a prototype -or- use a hardware emulator?

2) Prototype in FPGA (if you considering using an ASIC* in the final product)

Hardware design is migrating from board level products to "Systems on a Chip" and FPGA* designs. The High level Design Languages (HDL's) are providing for greater re-usability and the generation of HDL "cores". More and more often these cores are being resold as "intellectual property". Your hardware design, (either ASIC, FPGA, or PCB)* should be developed with this in mind.

*ASIC = Application Specific Integrated Circuit
*FPGA = Field Programmable Gate Array
*PCB = Printed Circuit Board

Visit http://www.amontec.com for last document release and new Chameleon POD configuration
6  MISCELLANEOUS

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6.3  BIBLIOGRAPHY
1.  XCR3128XL 128 Macrocell CPLD, DS017 (v1.5) April 19, 2001, Xilinx.
(http://www.xilinx.com)

6.4  DOCUMENT INFORMATION
•  Author          "Laurent Gauch"
•  Filename        "amt_chm_specification.doc"

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